Notice of Allowability	Application No.	Applicant(s)	
	10/072,415	LEE ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 6/28/07*.

2. ☒ The allowed claim(s) is/are *74,75,77-81,83-86,88,89,92,102-106,108,109,111,113,114,116,118,120-127,132 and 133*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to independent claims 79, 83, 89 and 116 have been fully considered and are persuasive. The rejection of independent claims 79, 83, 89 and 116 has been withdrawn.

Allowable Subject Matter

2. Claims 74, 75, 77-81, 83-86, 88, 89, 92, 102-106, 108, 109, 111, 113, 114, 116, 118, 120-127, 132 and 133 are allowed.

3. The following is an examiner's statement of reasons for allowance: a search of the prior art failed to disclose or reasonably suggest a method of fabricating a field effect transistor with an emitter comprising providing a gate dielectric over a channel region, providing a gate over the gate dielectric and polishing the gate dielectric and gate material to form a gate aligned with the channel region, as recited in independent claim 74.

A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field effect transistor comprising providing a plurality of semiconductive regions adjacent to a channel region of a semiconductive material, wherein at least one of the semiconductor regions comprises an emitter; self-aligning a gate with the semiconductive regions after the providing the semiconductive regions; and providing gate dielectric material over the channel region and the gate dielectric material including an upper surface substantially elevationally coincident with an upper surface of the gate, as recited in independent claim 79.

A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field emission device comprising providing a plurality of semiconductive regions adjacent to a semiconductive material, and wherein the providing the semiconductive regions comprises providing one of the semiconductive regions comprising a plurality of emitters; providing a gate intermediate the semiconductive regions; and wherein the providing the semiconductive regions comprises providing the semiconductive regions adjacent to opposing sides of a channel region of the semiconductive material, and wherein the semiconductive regions are elevationally above an uppermost surface of the semiconductive material, as recited in independent claim 83.

A search of the prior art also failed to disclose or reasonably suggest a method of operating a field emission device comprising providing a plurality of semiconductive regions adjacent to a channel region, and wherein at least one of the semiconductive regions comprises an emitter; controlling current flow intermediate the semiconductive regions within the channel region and controlling emission of electrons from the field emitter using a gate intermediate the semiconductive regions; wherein the providing the semiconductive regions comprises providing the semiconductive regions adjacent to semiconductive material comprising a thin film semiconductive layer; and wherein the semiconductive material comprises the channel region, wherein the providing the semiconductive regions comprises providing the semiconductive regions adjacent to opposing sides of the channel region, and wherein the s semiconductive regions are

elevationally above an uppermost surface of the semiconductive material, as recited in independent claim 89.

A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field effect transistor with an emitter comprising providing a gate over a channel region without the use of a mask over the gate material, as recited in independent claim 102.

A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field effect transistor comprising providing spaced semiconductive regions including a channel region positioned there between; providing gate material and gate dielectric material over the channel region; polishing the gate dielectric material and the gate material to form a gate intermediate the spaced semiconductive regions over the channel region; and wherein the providing the semiconductive regions comprises providing a drain comprising a field emitter, as recited in independent claim 108.

A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field effect transistor comprising providing semiconductive material including a channel region; providing a source semiconductive region and a drain semiconductive region adjacent to the channel region of the semiconductive material, and wherein the providing the drain semiconductive region comprises providing a plurality of emitters; providing gate dielectric material over the channel region; and providing a gate over the gate dielectric material and the channel region; and wherein the providing the source and drain semiconductive regions comprises providing the source and drain semiconductive regions adjacent to

opposing sides of the channel region of the semiconductive material, and wherein the source and drain semiconductive regions are elevationally above an uppermost surface of the semiconductive material, as recited in independent claim 116.

A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field emission device comprising providing a plurality of semiconductive regions adjacent a semiconductive material, one of the regions comprising an emitter, providing a gate intermediate the semiconductive regions, wherein providing the emitter comprises forming a tip of the emitter elevationally below an upper surface of the gate and an upper surface of another one of the semiconductive regions, as recited in independent claim 118.

A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field effect transistor comprising providing semiconductive material including a channel region; providing a plurality of semiconductive regions adjacent to the channel region of the semiconductive material, wherein at least one of the semiconductor regions comprises an emitter; self-aligning a gate with the semiconductive regions after the providing the semiconductive regions providing gate dielectric material over the channel region; providing gate material over the gate dielectric material; and wherein the self-aligning comprises polishing the gate dielectric material and the gate material, as recited in independent claim 132.

A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field emission device comprising providing semiconductive material; providing a plurality of semiconductive regions adjacent to the semiconductive material, and wherein the providing the semiconductive regions

comprises providing one of the semiconductive regions comprising a plurality of emitters; providing a gate intermediate the semiconductive regions; and wherein the providing one of the semiconductive regions comprising the emitters comprises forming a tip of one of the emitters elevationally below an upper surface of the gate and an upper surface of another one of the semiconductive regions, as recited in independent claim 133.

4. Itoh et al. '107, Hirano et al. '318, Kane '426, Kanemaru et al. '478, Itoh et al. '595 and Hofmann et al. '605 disclose methods of forming field effect transistors comprising an emitter formed on the drain of the transistor, but the references do not disclose the limitations set forth above.

Gardner et al. '894, Inaba '258 and Gardner et al. '025 disclose a method of forming a field effect transistor comprising a self-aligned gate formed by chemical-mechanical polishing, but the references do not disclose forming an emitter on the drain of the transistor.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven J. Fulk
Patent Examiner
Art Unit 2891

September 13, 2007

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